REMARKS

By this Supplemental Amendment, claims 32-33, 35-37, 39-40 and 42-44 have been amended and new claims 82-89 have been added. Accordingly, claims 1-3, 5-21, 23-26, 28-33, 35-40, 42-44 and 82-89 are pending in the present application.

Claims 32-33, 35-37, 39-40 and 42-44 have been amended so that the preambles of each of these claims correspond with the preamble of its respective independent claim.

New claims 82-89 are patentably distinguishable over U.S. Patent No. 6,392,913 to Sandhu, cited in the Office Action dated September 4, 2002, because each of independent claims 82, 84, 85, 86 and 89 recites a first memory access line (which is formed of a first conductive material), a layer of a second conductive material disposed on the first memory access line, and a layer of a variable resistance material disposed on the layer of the second conductive material. Independent claims 84 and 85 further recite a first dielectric layer material having a first window formed therein, with the first memory access line disposed in the first window, and a second layer disposed on the first memory access line and having a second window formed therein, with the layer of second conductive material formed in the second window on the first memory access line. These combination of elements as recited in the claims are not taught or suggested in Sandhu.

Sandhu discloses a structure in which a memory access line 14 is formed on a substrate, and an insulating layer 16 is formed on the memory access line 14. A receptacle 20 is "formed as an aperture or recess within insulating layer 16" and is "defined by sidewalls 22 and a bottom surface 24." *See* col. 4, lns. 1-8. Inside receptacle 20, a plurality of layers is stacked on the memory access line 14, starting with a layer of polysilicon 26 forming a diode, a layer of conductive material 42 on the polysilicon 26, a layer of chalcogenide material 44 on the conductive material 42, a diffusion barrier 46 on the

chalcogenide material 44, and a second memory access line 16 on the diffusion barrier (and the insulative layer 16).

Sandhu fails to teach or suggest a layer of a second conductive material disposed on the first memory access line, and a layer of a variable resistance material disposed on the layer of second conductive material, since in Sandhu the chalcogenide layer 44 (the variable resistance material) is separated from the first memory access line 14 by two layers, and not one, as is the case in Applicants' claims. More specifically, while the polysilicon layer 26 is disposed on memory access line 14 and may be considered to be a layer of conductive material different from the material of memory access line 14, the chalcogenide layer 44 is not disposed on the polysilicon layer 26. Similarly, while the chalcogenide layer 44 is disposed on carbon layer 42 (considered here to be a conductive material), carbon layer 42 is not disposed on the memory access line 14.

Additionally, Sandhu fails to teach or suggest a second dielectric layer, much less one disposed on the first memory access line and over the dielectric (insulating) layer 16, and further having a second window formed therein (in addition to the "window" defined by receptacle 20 formed in the dielectric layer 16) as recited in claims 84-85.

Since Sandhu does not disclose the layered structure recited in Applicants' new claims 82-89, these claims are patenably distinguishable over the same. Dependent claims 83 and 87-88 depend from independent claims 82 and 86, respectively, and are allowable over Sandhu for at least the same reasons attributable to the latter. In view of the foregoing, therefore, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Dated: February 13, 2003

Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

32. (Amended) The memory ~~cell~~, as set forth in claim 31, wherein the first line is embedded in the substrate.

33. (Amended) The memory ~~cell,~~ as set forth in claim 31, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.

35. (Amended) The memory ~~cell~~, as set forth in claim 31, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique.

36. (Amended) The memory ~~cell~~, as set forth in claim 31, wherein the second conductive material comprises at least one of silver and gold.

37. (Amended) The memory ~~cell~~, as set forth in claim 31, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

39. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the first line is embedded in the substrate.

39. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the first line is embedded in the substrate.

40. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.

42. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique.

43. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the second conductive material comprises at least one of silver and gold.

44. (Amended) The electronic device ~~memory cell~~, as set forth in claim 38, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.